USA Detector Interface

section 3.2.2.6 of the

USA
Central Electronics
Design Specification

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<u>USA Detector Interface (Section 3.2.2.6)</u>

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3.2.2.6 USA Detector Interface

3.2.2.6.1 Function

The USA Detector Interface shall process the science data and shall provide the data to the CE bus through a dual port memory interface. The USA Detector Interface shall provide an interface to a GPS time synchronizer such that science data events may be time tagged with a 1us resolution. The USA Detector Interface shall provide an interface to the USA Analog/Digital Mux card to control the operation of the card and to acquire data from the card. The USA Detector Interface card shall provide for the CE bus processor to write discrete control bits destined for the special processors. The USA Detector Interface contains an ADSP-2100 uP, with associated support hardware and software in order to provide the before mentioned functions.

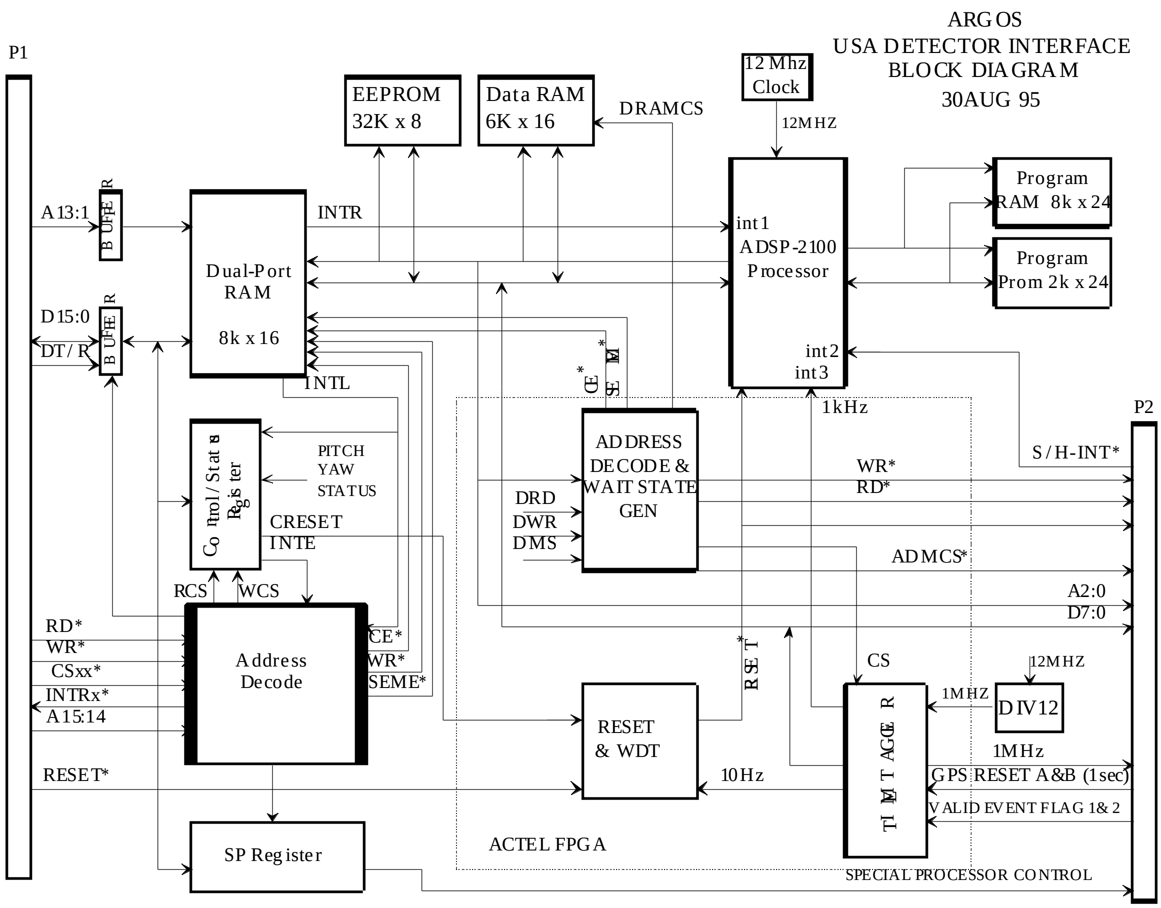


Figure 3.2.2.6.1-1 USA Detector Interface Block Diagram

The address map as seen by the Detector Interface CPU shall be as follows.

Program Memory

Address	Description
0000 - 07FF	Boot Memory PROM
2000 - 3FFF	Program RAM

Data Memory

Note that there exists two Data Memory mappings for the address segment 2000-3FFF depending on the state of bit 4, the EEPROM /Dual Port RAM Select bit, of the Interrupt Enable/EEPROM page register.

Address	Description	
0000-17FF	Data RAM	
1800-1807	A/D Mux Card Registers	
1A00	WDT Reset (Write Only)	
1A01	Interrupt Enable/EEPROM page register (Write)	
	bit 15	Watch dog timer enable
	bit 13	EEPROM Detector #2 interrupt enable
	bit 12	EEPROM Detector #1 interrupt enable
	bit 8	EEPROM Enable / Stop real-time timer
	bit 7	EEPROM Power enable off /on
	bit 4	EEPROM /Dual Port RAM Select
	bit 1	EEPROM Page select (MSB)
	bit 0	EEPROM Page select (LSB)
1C00	RH32 Shift Register LO (Write)	
1C00	Det 1 Time Tag Low (Read)	
1C01	Det 1 Time Tag High (Read)	
1C02	RH32 Shift Register High (Write)	
1C02	Det 2 Time Tag Low (Read)	
1C03	Det 2 Time Tag High (Read)	
1C04	Latch Current Timer Value (Write)	
1C04	Timer Register Low (Read)	
1C05	Timer Register High (Read)	
1C06	Set Seconds In Timer (Write)	
1C07	Status Register (Read)	
	bit 0	Shift Register Empty
	bit 1	D1 Time Tag Register Data Available
	bit 2	D2 Time Tag Register Data Available
1E00 - 1E07	Dual-Port RAM Semaphore Registers A - H	
	2000 - 3FFF	*Map Set for Dual Port RAM*
2000 - 3FFD	Dual-Port RAM	
3FFE	Status Register	
3FFF	Control Register (Interrupt to Detector Interface CPU)	
	2000 - 3FFF	*Map Set for EEPROM*
2000 - 3FFF	EEPROM page window (actual page selected by Interrupt Enable/EEPROM register)	

3.2.2.6.1.1 DIB Actel FPGA

The ARGOS USA Detector Interface board contains a sole Actel 1020A FPGA which is a 2000 gate equivalent device. One of the major functions of the FPGA is to provide board-level address decoding from the CE-bus and provide Program and Data Memory address decoding from the ADSP-2100 DSP. The Data Memory address decoding includes that for all FPGA-resident registers, such as the time-tag registers. A wait state generator is implemented for accessing the on-board EEPROM device (for non-volatile code storage) by inserting one extra cycle, or 333nS.

A second major function of the FPGA is to provide a 24-bit timer implemented as a 20-bit microsecond counter with a 4-bit second counter in its most significant nibble. The microsecond timer portion advances upon each tick of the 1MHz detector clock, and is reset upon the reception of a GPS synchronization pulse. The maximum count is (2^20-1) or 1,048,575 uS. The second portion of the counter advances on each GPS sync pulse to a maximum count of 15, and then rolls-over to zero. This counter section is reset only upon reset. Note that the GPS sync pulse input to the timer is preceded by a one-and-only-one flip-flop set to assure that the synchronization pulse is singular, thus independent of the pulse width of the GPS sync.

The FPGA also consists of time-tagger logic which complements the 24-bit timer by providing a means of storing the time at which valid events occur at each of the two detectors. Each of the two 24-bit time-tagger registers are independent, and are updated upon the reception of their respective detector valid event flag. The load enable to each of the registers is preceded by a one-and-only-one flip-flop set to assure that the event time is clocked in only once, at the start of the valid event. A third 24-bit register set provides a means for the DSP to determine the current time, since it is updated upon each detector clock cycle. Note that the DSP software must first disable the auto-increment of the register before reading it to assure its integrity.

The FPGA produces two interrupts to the ADSP2100, the valid event and the background interrupt. When a valid event is received from either of the two detectors and its respective interrupt mask is not set, then an interrupt will be issued to the ADSP2100 on IRQ3. Bit 9 of the 24-bit timer is used to generate a background interrupt every 1.024mS to the ADSP2100 on IRQ0. The background interrupt is not maskable.

A special processor interface consisting of a 32-bit parallel to serial interface, outputs a singular serial stream and strobe to the special processor at a 1 MHz rate. The DSP must first write the low 16-bit word, followed by the upper 16-bit word, to initiate the transfer sequence.

The reset circuit outputs a reset to FPGA-based logic and the ADSP2100 whenever any of the following conditions occur: a CPU reset is asserted on the CE-bus, the Control Register reset is asserted, or the watch dog timer has timed-out. The watch dog timer will time-out whenever a minimum interval of 131mS has expired without the DSP issuing a watch dog timer reset. Note that the watch dog timer enable bit must be set for proper operation. The pulse width of the watch-dog timer induced reset is approximately 2uS.

3.2.2.6.2 Physical Interface

The USA Detector Interface shall occupy a single bus slot within the USA.

3.2.2.6.3 CE Bus Interface

The USA Detector Interface shall contain a dual port memory interface and a control/status register interface to the CE bus. The dual port memory interface shall provide an 8k x 16 dual port RAM. Software protocols shall be employed to insure that the CE bus does not read or write the same location at the same time that the USA Detector Interface card may be reading or writing. The USA Detector Interface shall incorporate circuitry which will permit the CE processor to interrupt the USA Detector Interface processor and to permit the USA Detector Interface processor to interrupt the CE processor by implementing the interrupt capability of the dual port memory (The capability to interrupt the CE processor shall exist; however, the mechanism may not be utilized). The CE bus interrupt request level shall be jumper selectable and shall be enabled by an interrupt enable control bit in the control register. In addition, the USA Detector Interface shall provide the circuitry required to permit either processor to read and write the available semaphore registers available within the dual port memory. The USA Detector Interface card shall also provide a 16 bit register providing discrete TTL level control signals to the special processor cards. This register shall reset all bits to the low state when the CE bus reset signal is active. The address space as seen by the CE processor shall be as follows.

USA Detector Interface CE Bus Address Map
(Card Select = CS0B)

CE Byte Addr	CPU DM Word Addr	Length (16bit)	Description
0000-0001	2000	1	Science Data Register
0002-0041	2001-2020	32	State of Health Buffer ‘A’
0042-0081	2021-2040	32	State of Health Buffer ‘B’
0082-1541	2041-2AA0	2656	Telemetry Buffer ‘A’
1542-2A01	2AA1-3500	2656	Telemetry Buffer ‘B’
2A02-3EC1	3501-3F60	2656	Telemetry Buffer ‘C’
3EC2-3EFF	*3F61-3F7F*	*31*	*<Not Assigned>*
3F00-3F5F	3F80-3FAF	48	Debug Mode data
3F60-3F75	*3FB0-3FBA*	*11*	*<Not Assigned>*
3F76-3F79	3FBB -3FBC	2	DIB Application code date (Number of seconds since 1970)
3F7A-3FB9	3FBD-3FDC	32	Time & Attitude Data Buffer
3FBA-3FBB	3FDD	1	1 Second Sync Word Data Buffer
3FBC-3FFB	3FDE-3FFD	32	Command Data Buffer
3FFC-3FFD	3FFE	1	Status Register
3FFE-3FFF	3FFF	1	Control Register
400C-400D	1E06	1	Semaphore Register G (or 6)
400E-400F	1E07	1	Semaphore Register H (or 7)
8000-8001	-------	1	DIB Initialization Register
C000-C001	-------	1	Special Processor Discrete Control Register

The Dual Port interface utilizes three telemetry data buffers which permits the DIB not to have to wait for a free buffer when operating in the high-rate data mode. The DIB is capable of filling three buffers in _ second (at 20k events/second) , anotherwords each buffer can be filled in 1/6 sec. This buffer arrangement permits the CPU/1553 processor to service each buffer every 1/3 sec (in high-rate) while the DIB has sufficient buffer space.

3.2.2.6.3.1 CE Bus Interface Register Definitions

3.2.2.6.3.1.1 Science Data Register

The format of the Detector Interface’s Science Data register is as follows:

Science Register Definition 0000 Hex

Bit F	E	D	C	B	A	9	8
M3	**M2**	**M1**	**M0**	**WC11**	**WC10**	**WC9**	**WC8**
Bit 7	6	5	4	3	2	1	0
WC7	**WC6**	**WC5**	**WC4**	**WC3**	**WC2**	**WC1**	**WC0**

M3-M0 - Science Data Mode

The definition for the science data modes are as follows:

M3	M2	M1	M0	MODE DEFINITION	SD RATE
0	0	0	0	IDLE MODE	LOW
0	0	0	1	EVENT MODE 1	LOW
0	0	1	0	EVENT MODE 2	HIGH
0	0	1	1	EVENT MODE 3	LOW
0	1	0	0	EVENT MODE 4	HIGH
0	1	0	1	SPECTRAL MODE	LOW
0	1	1	0	RH PROCESSOR MODE	OFF
0	1	1	1	<not assigned>	--
1	0	0	0	LOW RATE SIM MODE	LOW
1	0	0	1	HIGH RATE SIM MODE	HIGH
1	0	1	0	<not assigned>	--
1	0	1	1	<not assigned>	--
1	1	0	0	<not assigned>	--
1	1	0	1	<not assigned>	--
1	1	1	0	<not assigned>	--
1	1	1	1	<not assigned>	--

WC11-WC0 - Science Buffer Word Count

Indicates the number of words (16-bit) that are in the telemetry buffer pointed to by the status register. The range is from 0 to 2656 (0xA60) words, which is the maximum buffer size. The word count is always updated at the same rate as the number of telemetry buffers used. Thus, in low rate telemetry, a single buffer is used; while at high rate telemetry, a total of three telemetry buffers are used.

3.2.2.6.3.1.2 Status Register

The format of the Detector Interface's Status register is as follows:

Status Register Definition 3FFC Hex (Semaphore 400C hex)

Bit F	E	D	C	B	A	9	8
SDV	**CME**	**STE**	**SOV**	**TB1**	**TB0**	**HA/B**	**HKA**
Bit 7	6	5	4	3	2	1	0
S7	**S6**	**S5**	**S4**	**S3**	**S2**	**S1**	**S0**

SDV Science Data Available, this bit when set indicates that the buffer pointed to by the A/B bit contains valid science data. This bit should be reset by the CPU/1553 processor when the buffer has been completely read.

CME Command Error, this bit when set indicates the DPC detected a command error. This bit should only be reset following a soft or hard reset of the DPC.

STE Self Test Error, this bit when set indicates that the DPC detected self test errors. This bit should only be reset by the DPC following a soft or hard reset.

SOV Science Data Overflow, this bit is set by the DPC if the SDV bit is still set when the next science data sample period begin or if the 1SEC command is not received by the DPC within an appropriate time. This bit should only be reset by the DPC following a soft or hard reset condition.

TB1:0 These bits are set by the DPC to indicate to the CPU/1553 processor to use the appropriate data buffer for science data.

TB1	TB0	TELEMETRY BUFFER
0	0	SCIENCE DATA IN 'A'
0	1	SCIENCE DATA IN 'B'
1	0	SCIENCE DATA IN 'C'
1	1	<ILLEGAL BUFFER SELECTION>

HA/B This bit is set by the DPC to indicate to the CPU/1553 processor to use the A housekeeping buffer for housekeeping data. If this bit is reset, the B housekeeping buffer should be used by the CPU/1553 processor.

HKA Housekeeping Data Available, this bit when set indicates that the housekeeping data sub-buffer pointed to by least significant 3 bits of the time code word received from the 1553 one second sync command plus one contains valid housekeeping data. This bit should be reset by the CPU/1553 processor when the buffer has been completely read. The DPC should update the sub-buffer within 500ms from the one second sync command. Remember, if the time code word received is 1 then housekeeping sub-buffer 2 should be updated so that the sub-frame is available for the 1553 interface before the next time code word is received.

S7:0 State Code bits 7:0, these bits describe the operational software state of the destination processor.

3.2.2.6.3.1.3 Control Register

The format of the Detector Interface's Control register is as follows:

Control Register Definition 3FFE Hex (Semaphore 400E hex)

Bit F	E	D	C	B	A	9	8
CAV	**OVF**	**1SEC**	**UPL**	**TAA**	**SRS**	**X**	**X**
Bit 7	6	5	4	3	2	1	0
X	**X**	**X**	**WC4**	**WC3**	**WC2**	**WC1**	**WC0**

CAV Command Available, this bit when set by the CPU/1553 processor indicates that a command or memory upload was loaded beginning at address 3FBC hex. This bit should be reset by the Destination Processor (DPC) after the command or memory upload has been removed from the command buffer area.

OVF Overflow, this bit when set by the CPU/1553 processor indicates that the CAV bit was still set when an attempt to load another command or memory upload was attempted.

1SEC One Second, this bit when set by the CPU/1553 processor indicates that the one second sync signal has been received from the 1553 interface and the associated data word was loaded at location 3FBA hex. This bit should be reset by the DPC when recognized by the interrupt generated as a result of the CPU/153 card write.

UPL Upload, this bit when set by the CPU/1553 processor shall command the DPC to the upload state. During the upload state, the DPC shall accept 1 to 32 word blocks of data through the command buffer (starting address 3FBC hex) from the CPU/1553 card. The CAV bit, and OVF bit if applicable, shall accompany each block transfer of the upload similar to the command protocol. The CPU/1553 will flush any existing commands and will inhibit further commanding to a DPC during a memory upload. The UPL bit shall remain set until a non-upload command is entered into the control register by the CPU/1553. This provides a means for the status of the upload to be observed by ground operations prior to the transfer of program execution to the uploaded program.

TAA Time/Attitude data available. this bit when set by the CPU/1553 processor indicates that the Time/Attitude buffer has been updated with data starting at address 3F7A hex.

SRS Soft Reset, this bit when set by the CPU/1553 processor shall command the DPC to the soft reset state. The DPC shall remain in the soft reset state until this bit is released by the CPU.

WC4:0 Word Count 4:0, indicates the number of words loaded into the command buffer for the command or memory upload; 1 = 1, 31 = 31, 0 = 32.

3.2.2.6.3.1.4 DIB Initialization Register

The DIB contains an Initialization Register that doubles as a control (write) or status (read) register. The control format is as follows:

Initialization Register Definition- Control 8000 Hex

Bit 7	6	5	4	3	2	1	0
LPB	**SP2**	**SP1**	**X**	**X**	**X**	**X**	**RST***

RST* Resets the entire Detector Interface when asserted low. Must be high for operation.

SP1 Spare Output #1 connected to pin 21C of P2 backplane.

SP2 Spare Output #2 connected to pin 22C of P2 backplane.

LPB Connects to bit 7 of the Initialization Register - Status format (loopback).

The status format of the Initialization register is as follows:

Initialization Register Definition- Status 8000 Hex

Bit 7	6	5	4	3	2	1	0
LPB	**SPI2**	**SPI1**	**PULK**	**PLK**	**YULK**	**YLK**	**DPR***

DPR* Dual Port Interrupt request pending when asserted low.

YLK Yaw Lock Indicator.

YULK Yaw Unlock Indicator.

PLK Pitch Lock Indicator.

PULK Pitch Unlock Indicator.

SPI1 Spare Input #1 connected to pin 19C of P2 backplane.

SPI2 Spare Input #2 connected to pin 20C of P2 backplane.

LPB Connects to bit 7 of the Initialization Register - Control format (loopback).

3.2.2.6.3.1.5 Special Processor Discrete Control Register

The DIB contains a Special Processor Discrete Control Register as defined by the following format:

Special Processor Discrete Control Register Definition **C000 Hex**

Bit F	E	D	C	B	A	9	8
X	**X**	**R3SMC**	**R3RS***	**R6SP2**	**R6SP1**	**R6RS***	**RHM7**
Bit 7	6	5	4	3	2	1	0
RHM6	**RHM5**	**RHM4**	**RHM3**	**RHM2**	**RHM1**	**RHM0**	**RHRS***

RHRS* RH32 Reset, Active Low
RHMx RH32 Mode

R6RS* R6000 Reset, Active Low
R6SP1 R6000 Spare 1
R6SP2 R6000 Spare 2

R3RS* RH3000 Reset, Active Low
R3SMC RH3000 Slave/Master Control

3.2.2.6.3.2 Detector Interface Commands

A summary of all USA DIB 1553 commands is illustrated in the two tables below. The first chart identifies those commands that are destined for the detector while the second chart identifies those for the Detector Interface.

USA Detector Interface Commands RT Address = 17, Function Code = 11

Command Destined for the Detector

Command Description	*Detector #1 Command*		*Detector #2 Command*		*Required Parameter Word*	
	Mnemonic	*Bit Pattern*	*Mnemonic*	*Bit Pattern*	*Bit Pattern*	*Description*
High voltage select converter A	UD1HVSA	9100	UD2HVSA	1110		
High voltage select converter B	UD1HVSB	1101	UD2HVSB	9111		
High voltage on	UD1HVON	1102	UD2HVON	9112		
High voltage off	UD1HVOFF	9103	UD2HVOFF	1113		
High voltage feedback hold	UD1HVHLD	1104	UD2HVHLD	9114		
High voltage feedback release	UD1HVREL	9105	UD2HVREL	1115		
Set high voltage level manual	UD1HVMAN	9106	UD2HVMAN	1116	10 LSBs	High voltage level
High voltage step up	UD1HVUP	1107	UD2HVUP	9117		
High voltage step down	UD1HVDWN	1108	UD2HVDWN	9118		
High voltage jump up (10 steps)	UD1HVJUP	9124	UD2HVJUP	1126		
High voltage jump down (10 steps)	UD1HVJDN	1125	UD2HVJDN	9127		
Solenoid power enable	UD1SOLEN	9128	UD2SOLEN	112A		
Solenoid power disable	UD1SOLDS	1129	UD2SOLDS	912B		
Gas purge enable	UD1PRGEN	9109	UD2PRGEN	1119		
Gas purge maximum duration	UD1PRGSM	910A	UD2PRGSM	111A		
Gas purge off	UD1PRGOF	110B	UD2PRGOF	911B		
Gas purge on timed	UD1PRGST	910C	UD2PRGST	111C	5 LSBs	Gas purge time
Calibrate maximum duration	UD1CALSM	110D	UD2CALSM	911D		
Calibrate off	UD1CALOF	110E	UD2CALOF	911E		
Calibrate on timed	UD1CALST	910F	UD2CALST	111F	5 LSBs	Calibrate on time
Enable valid event flag & data	UD1VEFON	1120	UD2VEFON	9122		
Disable valid event flag & data	UD1VEFOF	9121	UD2VEFOF	1123		
Detector Science Data Test	UD1SCTST	91F5	UD2SCTST	91F6		

Command Destined for the Detector Interface

Command	DIB Command		Required Parameter Word	
Description	***Mnemonic***	***Bit Pattern***	***Bit Pattern***	***Description***
Set VEF/PH time threshold	UTIMETHR	11DF	6 LSBs	Time threshold value (0 to 3F hex) in uS. Initialized to 40uS (28 hex) upon DIB power-up
Enable serial data to RH Processor	URHSDEN	91D1		
Disable serial data to RH Processor	URHSDDIS	11D0		
Select science mode #1 (Event mode #1)	USCIMD1	91E1		
Select science mode #2 (Event mode #2)	USCIMD2	91E2		
Select science mode #3 (Event mode #3)	USCIMD3	11E3		
Select science mode #4 (Event mode #4)	USCIMD4	91E4		
Select science mode #5 (Spectral mode)	USCIMD5	11E5		
Select science mode #6 (RH Processor mode)	USCIMD6	11E6		
Select science mode #7 (unassigned)	USCIMD7	91E7		
Select science mode #8 (Low rate sim mode)	USCIMLO	91E8		
Select science mode #9 (High rate sim mode)	USCIMHI	11E9		
Start simulated data mode	USIMSRT	11F1		
End simulated data mode	USIMEND	91F0		
Save program to EEPROM	UDPROMSV	11F2		
Soft reset	UDSRST	1180		
Dump Data RAM	UDDMPDRAM	1191		
Dump I/O map	UDDMPIO	1192		
Dump program RAM	UDDMPPRAM	1194		
Dump program ROM	UDDMPPROM	9195		
Dump program EEPROM	UDDMPEE	9196		

3.2.2.6.3.3 Detector Interface Protocol

The CPU/1553 card software is designed such that commands to other processor cards will not be sent any faster than one every 20ms. It is the responsibility of the destination processor therefore to receive commands at a faster rate than this. As will be seen in the following protocol, if a command is still resident in a destination processor's command buffer area, and the CPU/1553 card sends another command, the CPU/1553 card will overwrite the command buffer and will set a command overflow status bit. The CPU/1553 is expected to flush all queued commands and to prevent any further commanding during a memory upload to a dual port memory based sub-process. However, 1553 one second sync commands are expected to continue to occur.

Location 3FFE hex of the standard dual port memory interface shall be defined as a control register and location 3FFC shall be defined as a status register with respect to the CPU/1553 card. Semaphore location 400E shall be defined as the controlling semaphore for access to the control and semaphore location 400C shall be the controlling semaphore for access to the status register.

Command or Memory Upload Programming Example

CPU/1553 Card	Destination Processor Card
- CPU card determines command to be sent to DPC - CPU Masks Interrupts - CPU card requests DPC command buffer semaphore by writing a 0000 hex to location 400Eh and waits up to 25us minimum for the memory to become available, i.e., reading a value of 0000 hex at location 400Eh. - CPU reads control register to verify that the command available bit was reset in control register - CPU releases semaphore - CPU enables interrupts - CPU writes command or upload into command buffer starting at address location 3FBC hex, up to 32 words - CPU Masks Interrupts - CPU card requests DPC command buffer semaphore by writing a 0000 hex to location 400Eh and waits up to 25us minimum for the memory to become available, i.e., reading a value of 0000 hex at location 400Eh. - CPU sets command available bit in control register and overflow bit in control register if semaphore memory request time-out or if command available bit was set in control register, and set UPL bit if operation is a memory upload, generates interrupt to DPC - CPU releases semaphore - CPU enables interrupts	
	- DPC receives control register write interrupt - DPC card requests command buffer semaphore by writing a 0000 hex to location 400Eh and waits up to 25us minimum for the memory to become available, i.e., reading a value of 0000 hex at location 400Eh. - DPC reads control register to verify that the command available bit was set and the upload and overflow bit status. - DPC releases command buffer semaphore - DPC reads command or upload from command buffer starting at address location 3FBCh, up to 32 words - DPC card requests command buffer semaphore by writing a 0000 hex to location 400Eh and waits up to 25us minimum for the memory to become available, i.e., reading a value of 0000 hex at location 400Eh. - DPC resets command available bit in control register. - DPC releases command buffer semaphore

Science Data Acquisition Programming Example

CPU/1553 Card	Destination Processor Card
	- DPC initially writes first block of science data to buffer A
	- DPC requests command buffer semaphore
	- DPC sets SDAV and A/B flag
	- DPC releases command buffer semaphore
- CPU Masks Interrupts	
- CPU card requests DPC command buffer semaphore	
- CPU reads status register to verify if SDAV bit is set and A or B availability	
- CPU releases semaphore	
- CPU enables interrupts	
- if science data available, CPU reads science data	
	- while CPU reads buffer A, DPC generates buffer B
- When done reading buffer A, CPU Masks Interrupts	
- CPU card requests DPC command buffer semaphore	
- CPU resets SDAV bit is set in status register	
- CPU releases semaphore	
- CPU enables interrupts	
	- DPC requests command buffer semaphore
	- DPC reads status, and if SDAV bit reset then set SDAV bit and reset A/B bit.
	- DPC releases command buffer semaphore
Process repeats	

3.2.2.6.3.4 Telemetry Buffer Construction

The telemetry buffers of the Detector Interface board are constructed in accordance with either of two modes, the low rate and the high rate. The low rate utilizes two of the three telemetry buffers, A and B, alternating construction between them at a one second rate. The high rate utilizes all three telemetry buffers (A, B and C) within the one second interval.

Each of the science data telemetry modes operates at either the low or high rate as shown in the table below. Note that the idle mode (upon power-up) is associated with the low output data rate in case the DIB is requested to execute the memory dump.

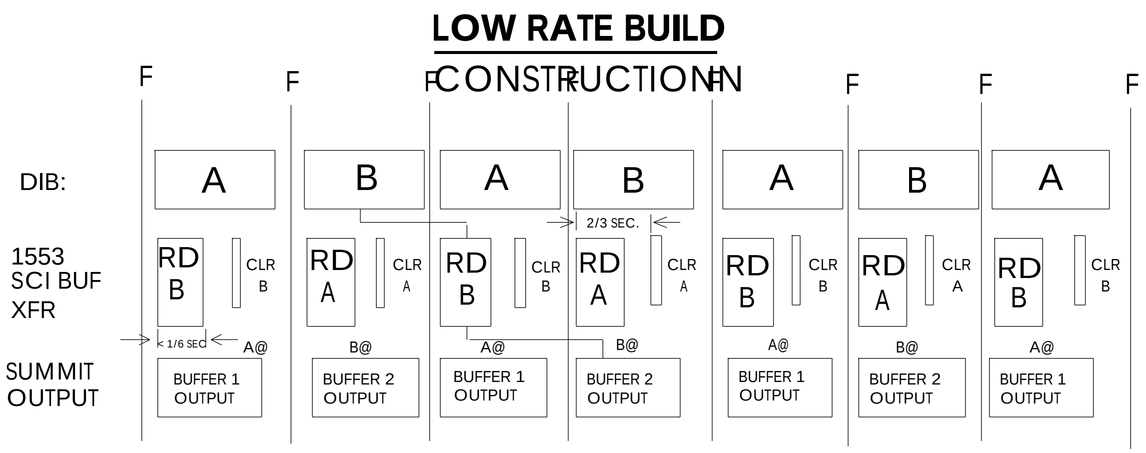
Science Data Telemetry Modes

Mode	*Definition*	*Rate*
0	Idle Mode	Low
1	Event Mode #1, 5-1-6 PEPs	Low
2	Event Mode #2, 5-1-6 PEPs	High
3	Event Mode #3, 4-1-10 PEPs	Low
4	Event Mode #4, 4-1-10 PEPs	High
5	Spectral Mode	Low
6	RH Processor Mode	Off
7	<Not Assigned>	N/A
8	Low Rate Simulation Mode	Low
9	High Rate Simulation Mode	High
10-15	<Not Assigned>	N/A

3.2.2.6.3.4.1 Low Rate

A diagram illustrating the telemetry buffer construction in the low rate is shown in the figure below. The low rate utilizes two of the three telemetry buffers, A and B, alternating construction between them at a one second rate upon each receipt of framesync (F). While the DIB is constructing a particular buffer, the opposite buffer is read by the CPU/1553 processor within the first 1/6 second of the framesync interval. At the 2/3 second mark, that buffer is then cleared (written to all zeroes) by the DIB in preparation for the next cycle. The Summit 1553 processor (located on the CPU/1553 assembly) will output the telemetry data in the following cycle which is two seconds behind the DIB's construction of the buffer.

03/06/95

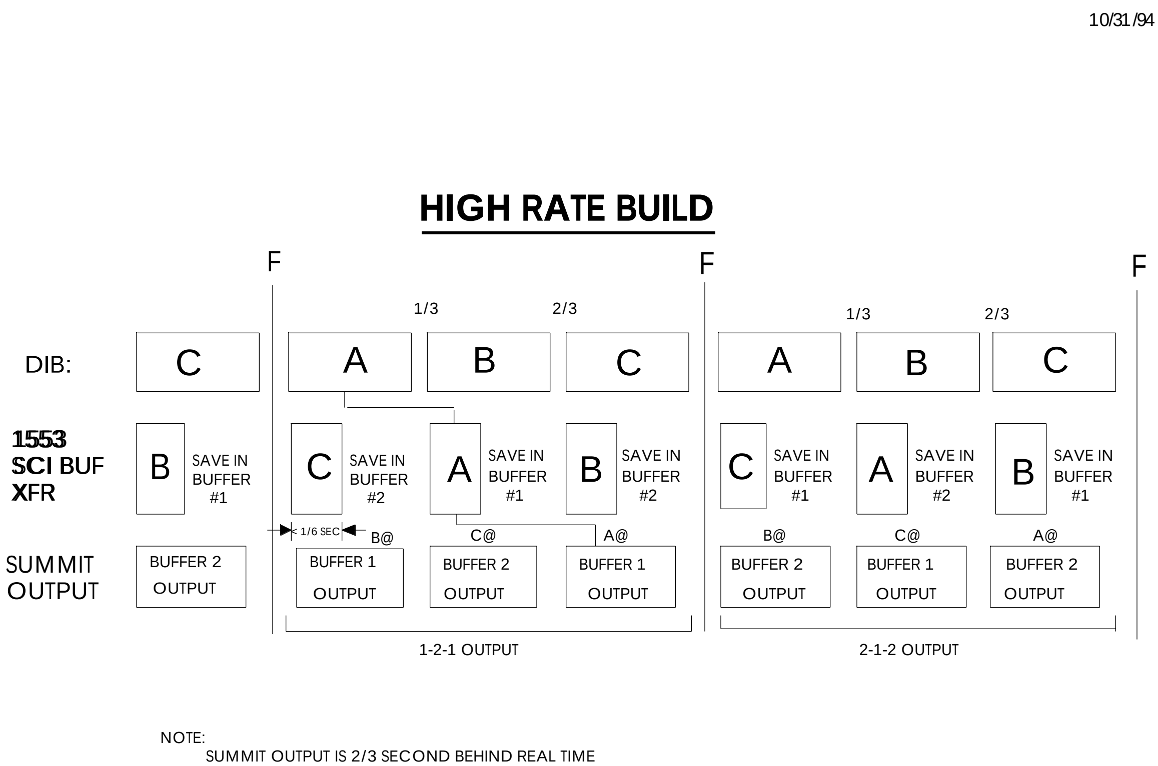


NOTES:

1. SUMMIT OUTPUT IS 2 SECONDS BEHIND REAL TIME
2. VERTICAL BAR ( ) REPRESENTS CLEAR OF BUFFER

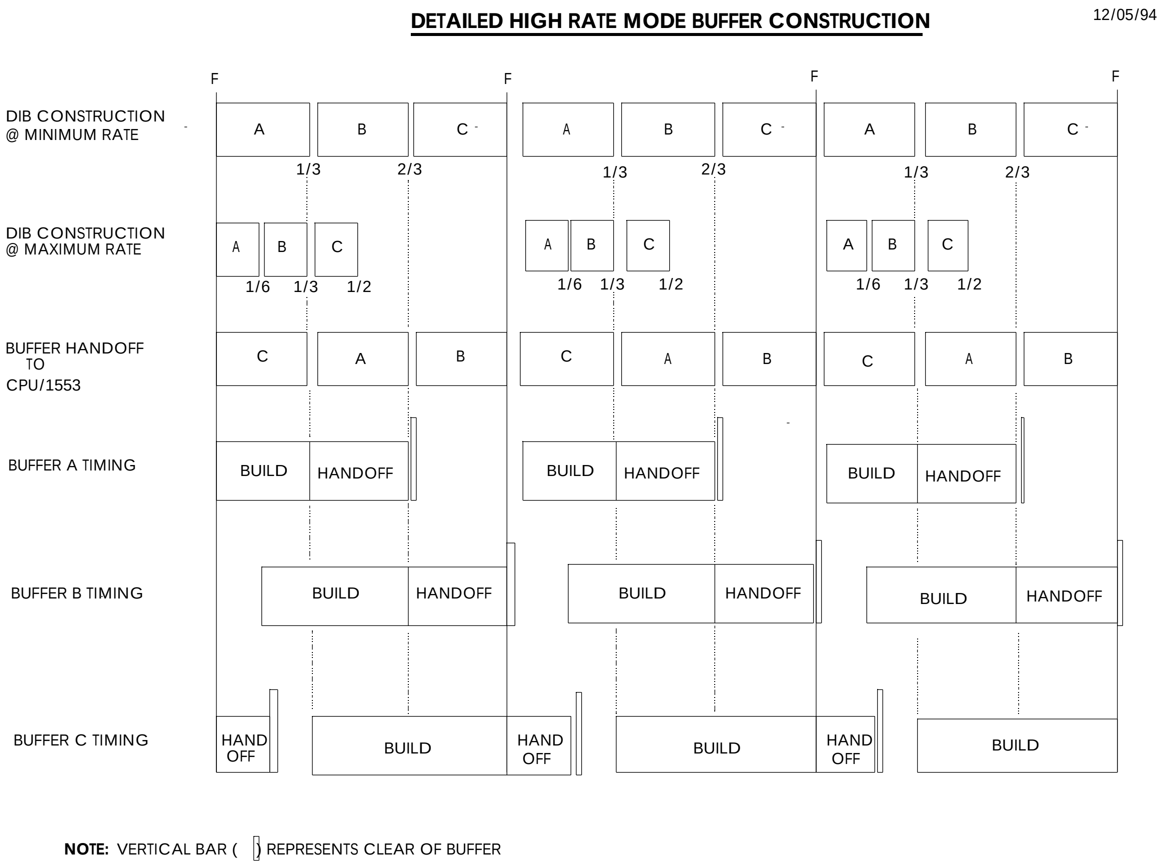
3.2.2.6.3.4.2 High Rate

A diagram illustrating the telemetry buffer construction in the high rate (with a relatively low input data rate) is shown in the figure below. Upon the receipt of framesync (F) the DIB begins construction of buffer A, and will continue to do so until the 1/3 second mark. At that time the DIB will begin construction of buffer B and the CPU/1553 will read the contents of buffer A, in less than 1/6 of a second. The B buffer will continue to be filled until the 2/3 second mark, when another buffer swap occurs. This time the DIB will initiate construction of the buffer C, while the CPU/1553 will read the contents of buffer B, again in less than 1/6 second. The C buffer will continue to be filled until the receipt of framesync. Note that in first 1/6 second period following framesync, buffer C will be read by the CPU/1553. The Summit 1553 processor (located on the 1553/CPU assembly) will output the telemetry data in a 1/3 second following the buffer read which is 2/3 seconds behind the DIB's construction of the buffer.



A second, more detailed diagram illustrating the telemetry buffer construction in the high rate is shown in the figure below. This figure attempts to illustrate the difference between buffer construction with a minimal input rate versus that when the input rate is at its maximum. The DIB at its maximum input data rate (20k events/second) is capable of filling all three buffers in only _ second. Thus, the DIB can fill each buffer in 1/6 second as opposed to the 1/3 second rate at which the CPU/1553 reads the data.

The first two lines of the figure illustrates the DIB's buffer construction at the minimal and maximum rates respectively. Since the buffer hand-off times to the CPU/1553 are fixed, buffer A may be built anytime within the first 1/3 second while the construction of both buffers B and C results in a elongated "build window". Buffer B can be built starting at the 1/6 second mark, while buffer C at the 1/3 second mark.



3.2.2.6.3.5 Science Data Modes

The science data modes consist of four event modes, the spectral mode, and two simulation modes. The science data modes and their associated telemetry rates are shown in section 3.2.2.6.3.4. The memory dump is also included which permits the DIB's program and data memory to be substituted in the science data.

3.2.2.6.3.5.1 Event Modes (USCIMD1 to USCIMD4)

The DIB may operate in any one of four science data event modes. The merits of each of the event modes is summarized in the table below.

Event Mode	Telemetry Data Rate	Maximum Events/second	Pulse Height Resolution	Time Stamp Resolution
#1	78 blocks/sec (low)	3070 events/sec	5-bit	6-bit (32uS)
#2	250 blocks/sec (high)	9950 events/sec	5-bit	6-bit (32uS)
#3	78 blocks/sec (low)	2456 events/sec	4-bit	10-bit (2uS)
#4	250 blocks/sec (high)	7960 events/sec	4-bit	10-bit (2uS)

Note that the odd numbered event modes operate at the low rate telemetry mode, while the even operate at the high rate. Event modes #3 and #4 have a much greater time stamp resolution (2 microseconds) then modes #1 and #2 (32 microseconds) but consequently contain less events per one second frame. Since there exists a great deal of similarity between the event modes, only event mode #1 will be discussed in detail, although the science data formats for each of the modes will be presented.

The science data format of event mode #1 is illustrated in the figure below. The format consists of 78 blocks of data with the first block dedicated for housekeeping data. The last two vectors of block #78 contain the science parameter block described in section 3.2.2.6.3.5.5. With the absence of the housekeeping block, a total of 77 blocks are constructed in the telemetry buffers. Event mode #1 uses a 5-1-6 photon event packet (PEP) with 5 bits dedicated for pulse height, one bit detector ID, and six bits of time (as shown in the figure).

When the “Start Simulated Data Mode” command (USIMSRT) is executed, a test data pattern is used in lieu of the detector stimulus. The pattern consists of a pulse height field that increments from zero to 19 thereby identifying the packet number. The detector ID alternates with all even packets identifying detector #1, and all odd packets identifying detector #2. The simulated pattern is shown in the table below:

PACKET NUMBER	***PULSE HEIGHT (5-bit)***	***DET ID (1-bit***	***TIME (6-bit)***
#0	00000	0	1010 00
#1	00001	1	0101 00
#2	00010	0	1010 00
#3	00011	1	0101 00
#4	00100	0	1010 00
#5	00101	1	0101 00
#6	00110	0	1010 00
#7	00111	1	0101 00
#8	01000	0	1010 01
#9	01001	1	0101 01
#10	01010	0	1010 01
#11	01011	1	0101 01
#12	01100	0	1010 01
#13	01101	1	0101 01
#14	01110	0	1010 01
#15	01111	1	0101 01
#16	10000	0	1010 10
#17	10001	1	0101 10
#18	10010	0	1010 10
#19	10011	1	0101 10

The contents of telemetry buffer A while in simulation data mode is shown below. Note that the contents of each block are identical except for the block time (underlined byte) which is incremented on each block. All 3-bits of the vector time field are set high. Telemetry buffer B is identical to buffer A except that the CE bus base address is B1542 in lieu of B0082.

DUAL PORT ADDR	BUFFER CONTENTS							
B0080:	XXXX	**00E0**	**501A**	**8250**	**3A84**	**51CB**	**50CA**	**0F51**
B0090:	**0A53**	**57A9**	**4AEA**	**B14B**	**6AB9**	**4F7D**	**582A**	**8D69**
B00A0:	**2A9D**	**6E05**	**01A8**	**2503**	**A845**	**1CB5**	**0CA0**	**F510**
B00B0:	**A535**	**7A94**	**AEAB**	**14B6**	**AB94**	**F7D5**	**82A8**	**D692**
B00C0:	**A9D6**	01E0	501A	8250	3A84	51CB	50CA	0F51
B00D0:	0A53	57A9	4AEA	B14B	6AB9	4F7D	582A	8D69
B00E0:	2A9D	6E05	01A8	2503	A845	1CB5	0CA0	F510
B00F0:	A535	7A94	AEAB	14B6	AB94	F7D5	82A8	D692
B0100:	A9D6	02E0	501A	8250	3A84	51CB	50CA	0F51
B0110:	....	....						

An example of parsing the telemetry data into photon event packets is shown below using the buffer contents starting at address B0082. In the diagram below, the photon event packet is represented as:

|------------x-------------|

where the left portion represents the 5-bit pulse height field; the X represents the single detector ID bit; the right hand portion represents the 6-bit time field.

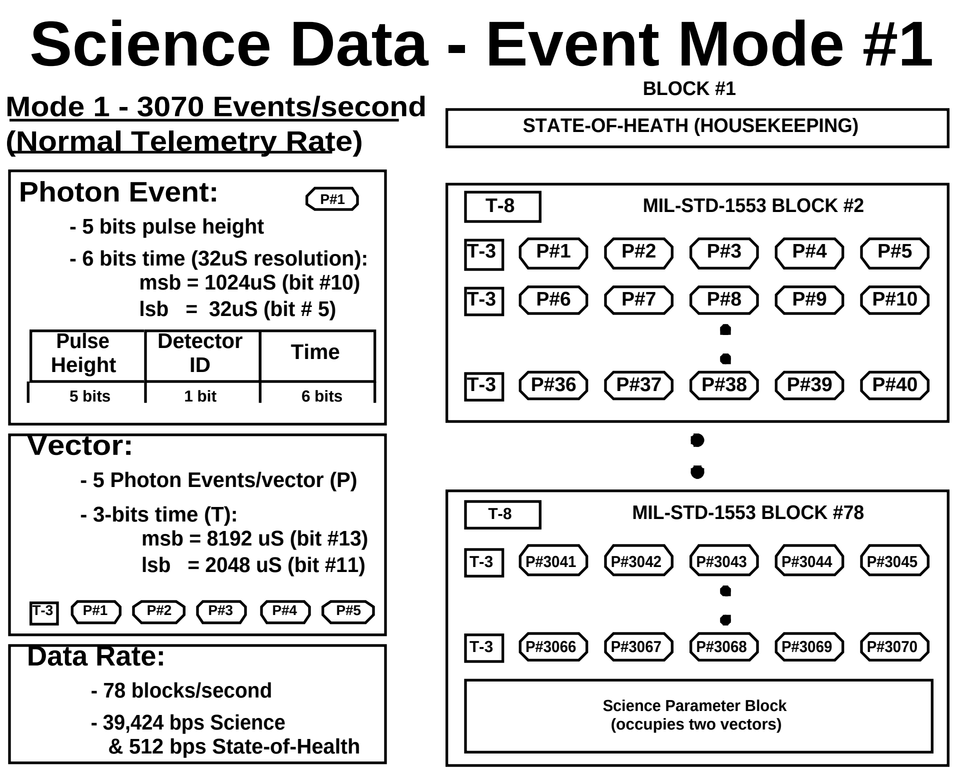
```
DUAL PORT ADDR                      BUFFER CONTENTS

HEXADECIMAL:
B0080:         XXXX  00E0   501A   8250   3A84   51CB   50CA   ....

BINARY:
B0082:         0000  0000   1110   0000          0101   0000   0001   1010
                  BLOCK     |VECT|--------------------------------------X-------------------|-----------------------X----
----
                                                PEP #0                        PEP #1

B0086:         1000  0010   0101   0000          0011   1010   1000   0100
                 -------|------------------------X--------------------|---------------------------------------X-------------------|-------
---------
                              PEP #2                                  PEP #3

B008A:         0101  0001   1100   1011          0101   0000   1100   1010
                X-------------------|  VECT |-------------------X-----------------------------------------|-----------------X--------
------ ...
               PEP #4                    PEP #5                      PEP #6
```



Science Data - Event Mode #2

Mode 2 - 9950 Events/second
(High Telemetry Rate)

Photon Event: P#1

- 5 bits pulse height
- 6 bits time (32uS resolution):
  msb = 1024uS (bit #10)
  lsb = 32uS (bit # 5)

Pulse Height	Detector ID	Time
5 bits	1 bit	6 bits

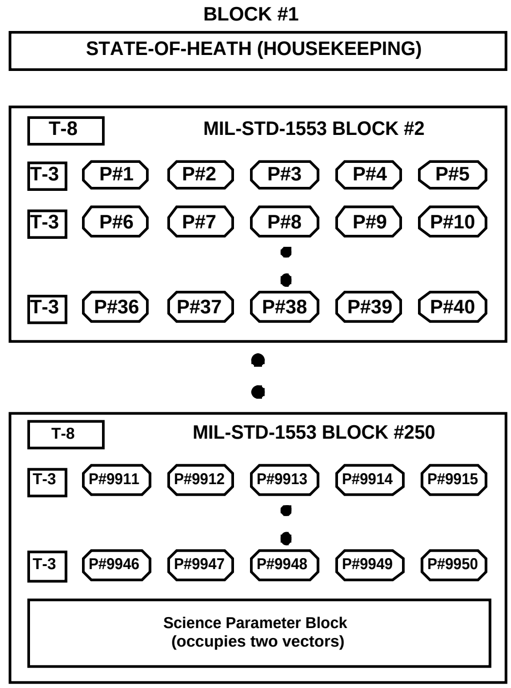
Vector:

- 5 Photon Events/vector (P)
- 3-bits time (T):
  msb = 8192 uS (bit #13)
  lsb = 2048 uS (bit #11)

T-3 P#1 P#2 P#3 P#4 P#5

Data Rate:

- 250 blocks/second
- 127,488 bps Science
  & 512 bps State-of-Health



Science Data - Event Mode #3

Mode 3 - 2456 Events/second
(Normal Telemetry Rate)

Photon Event: P#1

- 4 bits pulse height
- 10 bits time (2uS resolution):
  msb = 1024uS (bit #10)
  lsb = 2uS (bit # 1)

Pulse Height	Detector ID	Time
4 bits	1 bit	10 bits

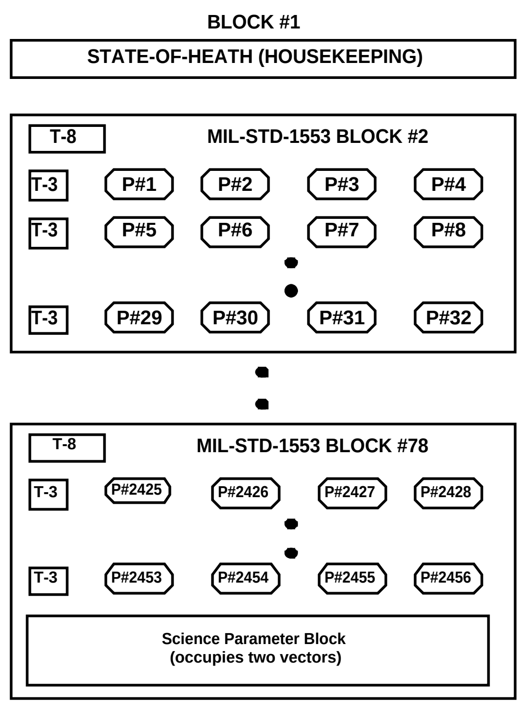
Vector:

- 4 Photon Events/vector (P)
- 3-bits time (T):
  msb = 8192 uS (bit #13)
  lsb = 2048 uS (bit #11)

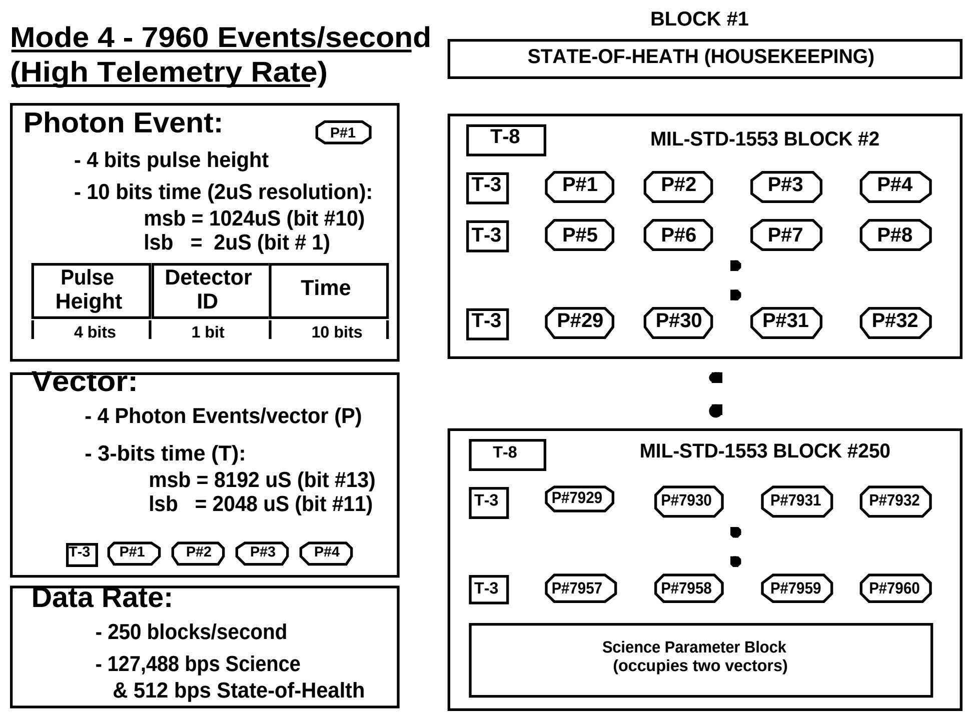
T-3 P#1 P#2 P#3 P#4

Data Rate:

- 78 blocks/second
- 39,424 bps Science
  & 512 bps State-of-Health



Science Data - Event Mode #4



3.2.2.6.3.5.2 Spectral Mode (USCIMD5)

The science data format for the spectral mode consists of 78 blocks of data with the first block dedicated for housekeeping data. With the absence of the housekeeping block, a total of 77 blocks will be constructed in the telemetry buffers. The two vectors (16 words) of the last block contain the GPS time, attitude information, detector counts, etc. as illustrated in the science parameter block figure described in section 3.2.2.6.3.5.5. Note that the spectral mode uses the same science parameter block as the event modes.

The spectral mode science data consists of 100 register sets, each containing 24 registers as described in the “Spectral Mode Register Set” figure below. Each register set corresponds to the received spectrum during a 10mS period. A framesync interval of one second requires 100 register sets, or 2400 words of science data (without the science parameter block). The register set is equally divided with the low byte of each word allocated to detector 1, and the high byte allocated to detector 2. Each detector contains 48 channels: the first 24 are 5-bits wide, the remaining 24 are 3-bits wide.

SPECTRAL MODE REGISTER SET

	DETECTOR #2		***DETECTOR #1***	
	15 13	12 8	7 5	4 0
WORD 0	CHAN 24	CHAN 0	CHAN 24	CHAN 0
WORD 1	CHAN 25	CHAN 1	CHAN 25	CHAN 1
WORD 2	CHAN 26	CHAN 2	CHAN 26	CHAN 2
WORD 3	CHAN 27	CHAN 3	CHAN 27	CHAN 3
WORD 4	CHAN 28	CHAN 4	CHAN 28	CHAN 4
WORD 5	CHAN 29	CHAN 5	CHAN 29	CHAN 5
WORD 6	CHAN 30	CHAN 6	CHAN 30	CHAN 6
WORD 7	CHAN 31	CHAN 7	CHAN 31	CHAN 7
WORD 8	CHAN 32	CHAN 8	CHAN 32	CHAN 8
WORD 9	CHAN 33	CHAN 9	CHAN 33	CHAN 9
WORD 10	CHAN 34	CHAN 10	CHAN 34	CHAN 10
WORD 11	CHAN 35	CHAN 11	CHAN 35	CHAN 11
WORD 12	CHAN 36	CHAN 12	CHAN 36	CHAN 12
WORD 13	CHAN 37	CHAN 13	CHAN 37	CHAN 13
WORD 14	CHAN 38	CHAN 14	CHAN 38	CHAN 14
WORD 15	CHAN 39	CHAN 15	CHAN 39	CHAN 15
WORD 16	CHAN 40	CHAN 16	CHAN 40	CHAN 16
WORD 17	CHAN 41	CHAN 17	CHAN 41	CHAN 17
WORD 18	CHAN 42	CHAN 18	CHAN 42	CHAN 18
WORD 19	CHAN 43	CHAN 19	CHAN 43	CHAN 19
WORD 20	CHAN 44	CHAN 20	CHAN 44	CHAN 20
WORD 21	CHAN 45	CHAN 21	CHAN 45	CHAN 21
WORD 22	CHAN 46	CHAN 22	CHAN 46	CHAN 22
WORD 23	CHAN 47	CHAN 23	CHAN 47	CHAN 23

The spectrum is quantified by taking the six MSBs of the pulse height to derive 64 channels, and then distributing them into 47 bins. The first 30 bins contain one channel per bin, while the remaining 17 contain 2 channels per bin. Each time a pulse height is received, the corresponding bin is incremented (but not past the maximum value) in the current register set. Every 10mS a new register set is used, up to the maximum of 100 sets (for a one second period).

An example of a science buffer containing spectral mode data is shown in the figure below. Note that the buffer is first parsed into 24 word register sets to identify the channel fields for both detectors. (The first and third register sets are shown in bold type below). The example below assumes telemetry buffer A at CE bus address B0082 is the current buffer. The processing of telemetry buffer B is identical to buffer A except that the CE bus base address is B1542.

DUAL PORT ADDR	BUFFER CONTENTS							
B0080:	XXXX	**1F1F**	**3E3E**	**5D5D**	**7C7C**	**9B9B**	**BABA**	**D9D9**
B0090:	**F8F8**	**1717**	**3636**	**5555**	**7474**	**9393**	**B2B2**	**D1D1**
B00A0:	**F0F0**	**0F0F**	**2E2E**	**4D4D**	**6C6C**	**8B8B**	**AAAA**	**C9C9**
B00B0:	**E8E8**	1F1F	3E3E	5D5D	7C7C	9B9B	BABA	D9D9
B00C0:	F8F8	1717	3636	5555	7474	9393	B2B2	D1D1
B00D0:	F0F0	0F0F	2E2E	4D4D	6C6C	8B8B	AAAA	C9C9
B00E0:	E8E8	**1F1F**	**3E3E**	**5D5D**	**7C7C**	**9B9B**	**BABA**	**D9D9**
B00F0:	**F8F8**	**1717**	**3636**	**5555**	**7474**	**9393**	**B2B2**	**D1D1**
B0100:	....	....						

An example of parsing the spectral telemetry data into histogram data is shown below using the buffer contents starting at address B0082.

DUAL PORT ADDR BUFFER CONTENTS

HEXADECIMAL:

B0080:	XXXX	**1F1F**	**3E3E**	**5D5D**	**7C7C**	**9B9B**	**BABA**	**D9D9**	**F8F8**
		WD 0	WD 1	WD 2	WD 3	WD 4	WD 5	WD 6	WD 7

|---------------------PART OF FIRST REGISTER SET - 0 TO 10mS----------------------
----|

* *
* *
* *

B00B0:	**E8E8**	1F1F	3E3E	5D5D	7C7C	9B9B	BABA	D9D9	F8F8
	WD 23	WD 0	WD 1	WD 2	WD 3	WD 4	WD 5	WD 6	WD 7

|--------------------PART OF SECOND REGISTER SET - 10 TO 20mS------------------
----|

The register sets can be further reduced to retrieve the spectrum as follows:

BINARY:

B0082: 0001 1111 0001 1111 First register set, word 0
|CH24|-----CH 0-----| |CH24|----CH 0------|
|--DETECTOR #2--| |--DETECTOR #1--|

B0084: 0011 1110 0011 1110 First register set, word 1
|CH25|-----CH 1-----| |CH25|-----CH 1----|
|--DETECTOR #2--| |--DETECTOR #1-|

The example pattern corresponds to the following values for each of the 24 register sets:

DETECTOR #2	***DETECTOR #1***

	15 0	13 12	8 7	5 4
WORD 0	000	1 1111	000	1 1111
WORD 1	001	1 1110	001	1 1110
WORD 2	010	1 1101	010	1 1101
WORD 3	011	1 1100	011	1 1100
WORD 4	100	1 1011	100	1 1011
WORD 5	101	1 1010	101	1 1010
WORD 6	110	1 1001	110	1 1001
WORD 7	111	1 1000	111	1 1000
WORD 8	000	1 0111	000	1 0111
WORD 9	001	1 0110	001	1 0110
WORD 10	010	1 0101	010	1 0101
WORD 11	011	1 0100	011	1 0100
WORD 12	100	1 0011	100	1 0011
WORD 13	101	1 0010	101	1 0010
WORD 14	110	1 0001	110	1 0001
WORD 15	111	1 0000	111	1 0000
WORD 16	000	0 1111	000	0 1111
WORD 17	001	0 1110	001	0 1110
WORD 18	010	0 1101	010	0 1101
WORD 19	011	0 1100	011	0 1100
WORD 20	100	0 1011	100	0 1011
WORD 21	101	0 1010	101	0 1010
WORD 22	110	0 1001	110	0 1001
WORD 23	111	0 1000	111	0 1000

3.2.2.6.3.5.3 RH Processor Mode (USCIMD6)

The RH processor mode only outputs serial data to the Special Processor Data Interface; the DIB does not construct science data in this mode. The format of the transmitted data is that of the event mode's queue element as shown in section 3.2.2.6.8.1. Although the DIB does not generate science data in this mode, housekeeping data is generated.

3.2.2.6.3.5.4 Simulation Modes (USCIMLO and USCIMHI)

Two simulation modes, the low rate and high rate, fill the appropriate telemetry buffers entirely with a fixed test pattern to aid in debugging the system. The science parameter block is absent from the buffer in order to not disrupt the test pattern.

The test pattern definition for the low rate simulation mode is defined in the table below. Upon each framesync a different simulation pattern is selected from the four patterns below in order to assign unique values to each data word. The patterns are rotated through sequentially in the order shown. Buffer C is not used in the low rate mode and is consequently zeroed out.

Low Rate Simulation Mode

	Address Range	Simulation Patterns
Buffer A	0082 --> 1541	0000 --> 0A5F 4000 --> 4A5F 8000 --> 8A5F C000 --> CA5F
Buffer B	1542 --> 2A01	2000 --> 2A5F 6000 --> 6A5F A000 --> AA5F E000 --> EA5F
Buffer C	2A02 --> 3EC1	0000 --> 0000

The test pattern definition for the high rate simulation mode is defined in the table below. Upon each framesync a different simulation pattern is selected from the eight patterns in order to assign unique values to each data word. The patterns are rotated through sequentially in the order shown.

High Rate Simulation Mode

	Address Range	Simulation Patterns
Buffer A	0082 --> 1541	0000 --> 0A5F 2000 --> 2A5F 4000 --> 4A5F 6000 --> 6A5F 8000 --> 8A5F A000 --> AA5F C000 --> CA5F E000 --> EA5F
Buffer B	1542 --> 2A01	0A60 --> 14BF 2A60 --> 34BF 4A60 --> 54BF 6A60 --> 74BF 8A60 --> 94BF AA60 --> B4BF CA60 --> D4BF EA60 --> F4BF
Buffer C	2A02 --> 3EC1	14C0 --> 1F1F 34C0 --> 3F1F 54C0 --> 5F1F 74C0 --> 7F1F 94C0 --> 9F1F B4C0 --> BF1F D4C0 --> DF1F F4C0 --> FF1F

3.2.2.6.3.5.5 Science Parameter Block

Each of the four event modes and the spectral mode contain a science parameter block located at the last 16 words of the science data in accordance with the table below. (Note that the simulation modes defined in section 3.2.2.6.3.5.4 do not contain the block.)

Mode	***CE Address of start of Science Parameter Block***	***DIB DM Address of start of Science Parameter Block***
Low Rate	0x13A2 (Buffer A) *or* 0x2862 (Buffer B)	0x29D1 (Buffer A) *or* 0x3431 (Buffer B)
High Rate	0x3EA2 (Buffer C)	0x3F51 (Buffer C)

The block is created upon the receipt of framesync in the telemetry buffer currently in construction. In the low rate modes the block is located at the end of either buffers A or B, while in the high rate mode it is always located at the end of buffer C. The definition of each of the 16 words located in the block is as follows:

Word	***Variable Name***	***Description***
0	Mode (4 LSBs)	Defines the current science data mode. Remaining high order bits are not utilized.
1	GPS Week	Format: 0000 00kk kkkk kkkk ; LSB = 1 week
2	GPS Seconds (MSB)	Format: 0000 0000 0000 gggg
3	GPS Seconds (LSB)	Format: gggg gggg gggg gggg ; LSB = 1 second
4	GPS Microseconds (MSB)	Format: 0000 0000 0000 uuuu
5	GPS Microseconds (LSB)	Format: uuuu uuuu uuuu uuuu ; LSB = 1 microSec
6	Detector #1 Total Coincidence Count	Detector #1 Sensor’s Total Coincidence Count (UD1CTTCV) at the last housekeeping request.
7	Detector #2 Total Coincidence Count	Detector #2 Sensor’s Total Coincidence Count (UD2CTTCV) at the last housekeeping request.
8	Dump Flag (LSB)	LSB is high for dump frame; low for science data
9	Science Buffer A Word Count	The number of words in science buffer A at framesync. In the low rate this word count will be zero on alternating buffers.
10	Science Buffer B Word Count	The number of words in science buffer B at framesync. In the low rate this word count will be zero on alternating buffers.
11	Science Buffer C Word Count	The number of words in science buffer C at framesync. In the low rate this word count will always be zero.
12	DIB Detector #1 Event Count	The number of valid events the DIB received from detector #1 in the last framesync period.
13	DIB Detector #2 Event Count	The number of valid events the DIB received from detector #2 in the last framesync period.
14	Checksum	The checksum of all science words in all transmitted buffers whether low rate (A or B), or high rate (A, B and C).
15	Synchronization Pattern	Synchronization pattern (EB90) used for data reduction.

3.2.2.6.3.5.6 Memory Dump

The DIB will output dump memory data to substitute for the science data when requested by any UDDMPxxxx type command listed in section 3.2.2.6.3.2. The memory dump is indicated in the housekeeping telemetry via the 'DIB Flag and Dump Status register' as described in section 3.2.2.6.3.6 herein. Dump data may be requested while in any event mode (UDSCIMD1 to UDSCIMD4), spectral mode (UDSCIMD5) or the initial power-up state (mode 0) of the DIB. Dump data may not be requested in either simulation mode (USCIMLO or USCIMHI) or the RH Processor mode (USCIMD6), since the latter strictly outputs serial data to the Special Processor Data Interface.

The format of the memory dump is shown in the following figure.

MEMORY DUMP FORMAT		
WORD OFFSET	**DUMP FIELD**	**DESCRIPTION**
0	**EB90**	Synchronization Code
1	**BIT_FORMAT**	*Bit format of dump data:* **1616** = 16-bit format **2424** = 24-bit format
2	**DUMP_START_ADDR**	DIB Starting address of dump
3	**DUMP_MODE**	*DIB Command requesting dump data:* **1191** = Dump Data RAM (16-bit) **1192** = Dump I/O Map (16-bit) **1194** = Dump Program RAM (24-bit) **9195** = Dump Program ROM (24-bit) **9196** = Dump EEPROM (24-bit)
4	**WORD_COUNT**	Number of words to transfer. The bit format indicates the size of the word to transfer.
5	**<SPARE WORD>**	**0000** = Unused
6	**<SPARE WORD>**	**0000** = Unused
7 N	**DUMP DATA**	*Dump Data field arranged as either:* 1-1020 16-bit words *or* 1-680 24-bit words
N+1	**<SPARE WORD>**	**0000** = Unused

3.2.2.6.3.6 State-of-Health Telemetry

The DIB state-of-health telemetry is divided into two groups: the first consists of parameters that are updated in the telemetry downlink once per second, and the second, those that are updated once every sixteen seconds. The purpose of the following tables is to identify the parameters and their individual fields, not the parameter's specific location in the telemetry.

The following parameters are updated once per second, hence they are located in each of the 16 subframes of the state-of-health telemetry.

DIB State-of-Health Telemetry (Parameters updated each second)

BIT	MNEMONIC	DESCRIPTION	SET CONDITION	RESET CONDITION
0	SC0	STATE CODE BIT #0	N/A	N/A

1	SC1	STATE CODE BIT #1	N/A	N/A
2	SC2	STATE CODE BIT #2	N/A	N/A
3	SC3	STATE CODE BIT #3	N/A	N/A
4	SC4	STATE CODE BIT #4	N/A	N/A
5	SC5	STATE CODE BIT #5	N/A	N/A
6	SC6	STATE CODE BIT #6	N/A	N/A
7	SC7	STATE CODE BIT #7	N/A	N/A
8	D1_HV_FHLD_REL	Det #1 HV feedback hold (1) /free-running (0)	UD1HVHLD command issued	UD1HVREL command issued
9	D1_HV_SELCONVB	Det #1 HV module B powered.	UD1HVSB command issued	UD1HVSA command issued
10	D1_HV_SELCONVA	Det #1 HV module A powered.	UD1HVSA command issued	UD1HVSB command issued
11	D1_HV_ENABLE	Det #1 HV enabled	UD1HVON command issued	UD1HVOFF command issued
12	D1_PURGE_START	Det #1 gas purge start initiated	UD1PRGSM command issued	UD1CALOF or UD1PRGOF command issued
13	D1_PURGE_ENABL E	Det #1 gas purge enable initiated	UD1PRGEN command issued	UD1CALOF or UD1PRGOF command issued
14	D1_CALIB_START	Det #1 calibration start initiated	UD1CALSM command issued	UD1CALOF or UD1PRGOF command issued
15	D2_HV_FHLD_REL	Det #2 HV feedback hold (1) /free-running (0)	UD2HVHLD command issued	UD2HVREL command issued
16	D2_HV_SELCONVB	Det #2 HV module B powered.	UD2HVSB command issued	UD2HVSA command issued
17	D2_HV_SELCONVA	Det #2 HV module A powered.	UD2HVSA command issued	UD2HVSB command issued
18	D2_HV_ENABLE	Det #2 HV enabled	UD2HVON command issued	UD2HVOFF command issued
19	D2_PURGE_START	Det #2 gas purge start initiated	UD2PRGSM command issued	UD2CALOF or UD2PRGOF command issued
20	D2_PURGE_ENABL E	Det #2 gas purge enable initiated	UD2PRGEN command issued	UD2CALOF or UD2PRGOF command issued
21	D2_CALIB_START	Det #2 calibration start initiated	UD2CALSM command issued	UD2CALOF or UD2PRGOF command issued
22	DP_OVERFLOW_ ERROR	Dual port overflow - DIB built frame past 1.1mS mark due to absence of frame sync	Frame sync time-out occurred - detected by mS counter reaching 1100 mS in background ISR	Hard/Soft reset
23	QUEUE_FULL_ ERROR	DIB's photon event queue is full	DIB's 1023-element photon event queue is full in science/hkp ISR	Hard/Soft reset
24	COMMAND_ERROR	DIB detected a command error	DIB parsed an invalid command from the command data buffer in dual port ISR	Hard/Soft reset
25	ADC_TIMEOUT_ ERROR	A/D conversion time-out occurred on the A/D Mux board	Housekeeping data not received from A/D mux in background ISR	Hard/Soft reset
26	DET_CORR_ ERROR	Detector time & pulse height correlation error.	(Not implemented)	(Not implemented)
27	DET_HKP_ERROR	Detector housekeeping data not received by DIB	Housekeeping data not received from the detector in background ISR	Hard/Soft reset
28	SUBF_SYNC_ ERROR	DIB did not receive a frame sync	Frame sync time-out occurred - detected by mS counter reaching 1100 mS in background ISR	Frame sync is received
29	DP_OVERRUN_ ERROR	DIB dual port overrun - echo of the 8086 OVF flag of the control register	If the OVF & CAV flags are set in the dual port ISR	Hard/Soft reset
30	HKP_OVERRUN_ ERROR	Housekeeping overrun - DIB's A/B buffer was not serviced by the 8086.	If the HKA flag (of DIB status reg) is still set when a new frame is to be constructed in the background ISR	Hard/Soft reset
31	TIME_ATT_ ERROR	Time & attitude information was not updated in the last second.	Frame sync is received and time/attitude was not updated in the last second	Frame sync is received and time/attitude was updated in the last second

The following parameters are updated once every 16 seconds, hence they are located in only one of the 16 subframes of the state-of-health telemetry.

DIB State-of-Health Telemetry (Parameters updated once per 16 seconds)

DIB DUAL PORT CONTROL REGISTER (W/O WORD COUNT)		
BIT	**MNEMONIC**	**DESCRIPTION**
5	CAV	Command available bit
4	OVF	Overflow bit
3	SYN	One second sync bit
2	UPL	Memory upload bit
1	TAA	Time attitude data available bit
0	SRS	Soft reset bit

DIB SELF TEST ERROR REGISTER		
BIT	**MNEMONIC**	**DESCRIPTION**
9	SPARE1_ST	Bit definition is TBD
8	PWR_FAIL_ST	Selftest - power test failure
7	ADC_REF_FAIL_ST	Selftest - A/D reference failure
6	ADC_CONV_FAIL_ST	Selftest - A/D converter failure
5	DET_DATA_FAIL_ST	Selftest - detector data fail
4	DET_REPLY_FAIL_ST	Selftest - detector reply fail
3	RTI_FAIL_ST	Selftest - real time int fail
2	DATA_RAM_FAIL_ST	Selftest - data ram failure
1	DUAL_PORT_FAIL_ST	Selftest - dp ram failure
0	CPU_FAIL_ST	Selftest - cpu test failure

DIB DUAL PORT STATUS REGISTER (W/O STATE CODES)		
BIT	**MNEMONIC**	**DESCRIPTION**
7	SDV	Science data available bit
6	CME	Command error bit
5	STE	Self test error bit
4	SOV	Science data overflow bit
2-3	TB0:1	Telemetry buffer select *TB1 TB0* 0 0 buffer 'A' 0 1 buffer 'B' 1 0 buffer 'C' 1 1 <illegal>
1	HAB	Housekeeping A/B bit (A=1)
0	HKA	Housekeeping data available bit

DIB INTERRUPT ENABLE / EEPROM REGISTER		
BIT	**MNEMONIC**	**DESCRIPTION**
7	EEOFF	EEPROM power enable off(1) /on(0)
6	<Not utilized>	
5	WDTEN	Watch dog timer enable
4	PGSEL	EEPROM(1) /dual-port ram select
3	D2INTE	Detector 2 interrupt enable
2	D1INTE	Detector 1 interrupt enable
1	PG1	EEPROM page select (MSB)
0	PG0	EEPROM page select (LSB)

DIB FLAG & DUMP STATUS REGISTER		
BIT	**MNEMONIC**	**DESCRIPTION**
7	SIM_DATA_FLAG	Simulated data in use
6	SPARE2_FLAG	Bit definition is TBD
5	SPARE1_FLAG	Bit definition is TBD
4	DUMP_EEPROM	Dump - EEPROM in progress
3	DUMP_DATA_RAM	Dump - data ram in progress
2	DUMP_PROGRAM_RAM	Dump - program ram in progress
1	DUMP_PROGRAM_ROM	Dump - program prom in progress
0	DUMP_IO_MAP	Dump - io map in progress

DIB LAST PEP ADDRESS REGISTER		
BIT	**MNEMONIC**	**DESCRIPTION**
0-15	last_pep_addr	Last science buffer location a PEP was written in event modes. The valid range is from 0x2041 to 0x3F60.

DIB MILLISECOND COUNTER REGISTER (VALUE AT FRAMESYNC)		
BIT	**MNEMONIC**	**DESCRIPTION**
0-15	ms_counter	Contains the value of the millisecond counter at framesync. Each tic equals 1.024 mS. For a one second sync, the value should be approx. 0x3D0. Time-out occurs when the count equals 0x432 or approx. 1.1seconds, and consequently initiates the framesync task by default.

A/D MUX CONTROL REGISTER		
BIT	**MNEMONIC**	**DESCRIPTION**
7	DR2	Detector #2 reset
6	DR1	Detector #1 reset
5	HE2	Detector #2 housekeeping interrupt enable
4	SE2	Detector #2 science interrupt enable
3	HE1	Detector #1 housekeeping interrupt enable
2	SE1	Detector #1 science interrupt enable
1	LT	Loopback test
0	ASC	ADC start conversion strobe

A/D MUX STATUS REGISTER		
BIT	**MNEMONIC**	**DESCRIPTION**
7	C2E	Command data 2 empty
6	C1E	Command data 1 empty
5	SR2	Science data 2 ready
4	SR1	Science data 1 ready
3	HR2	Housekeeping data 2 ready
2	HR1	Housekeeping data 1 ready
1	SHI	Science/housekeeping interrupt pending
0	ACC	A/D conversion complete

A/D MUX MULTIPLEXOR REGISTER		
BIT	**MNEMONIC**	**DESCRIPTION**
7	<Not utilized>	Spare Bit
6	OEP	Odd/even command parity
5	ULS	Upper/lower 8-bit ADC data select
4	MS4	Mux address (MSB)
3	MS3	Mux address
2	MS2	Mux address
1	MS1	Mux address
0	MS0	Mux address (LSB)

3.2.2.6.3.7 Debug Register Definitions

The DIB's dual port interface includes a block of CE addressable memory (3F00 to 3F5F) which is assigned as debug mode data and contains registers useful in monitoring or debugging the DIB. Address space 3F30 to 3F5F is unimplemented and available for future growth. A list of the debug registers with their description and location follows.

Note: All bits are active high unless otherwise specified.

3F00: OPERATIONAL ERROR REGISTER		
BIT	**MNEMONIC**	**DESCRIPTION**
10-15	<Not utilized>	
9	TIME_ATT_ERROR	Time/Attitude not updated error
8	HKP_OVERRUN_ERROR	Housekeeping overrun - A/B buffer not serviced before new HKP done
7	DP_OVERRUN_ERROR	Dual_port overrun - new command received before previous completed
6	SUBF_SYNC_ERROR	Subframe sync not received error
5	DET_HKP_ERROR	Detector HKP data not received
4	DET_CORR_ERROR	Detector time/pulse ht correlation error
3	ADC_TIMEOUT_ERROR	A/D conversion time-out occurred
2	COMMAND_ERROR	Command error detected (CME)
1	QUEUE_FULL_ERROR	Photon event queue full
0	DP_OVERFLOW_ERROR	Dual-port overflow (SOV)

3F02: SELF TEST REGISTER		
BIT	**MNEMONIC**	**DESCRIPTION**
10-15	<Not utilized>	
9	SPARE1_ST	Bit definition is TBD
8	PWR_FAIL_ST	Selftest - power test failure
7	ADC_REF_FAIL_ST	Selftest - A/D reference failure
6	ADC_CONV_FAIL_ST	Selftest - A/D converter failure
5	DET_DATA_FAIL_ST	Selftest - detector data fail
4	DET_REPLY_FAIL_ST	Selftest - detector reply fail
3	RTI_FAIL_ST	Selftest - real time int fail
2	DATA_RAM_FAIL_ST	Selftest - data ram failure
1	DUAL_PORT_FAIL_ST	Selftest - dp ram failure
0	CPU_FAIL_ST	Selftest - cpu test failure

3F04: FLAG & DUMP MEMORY REGISTER		
BIT	**MNEMONIC**	**DESCRIPTION**
9-15	<Not utilized>	
8	EN_RH_OUT_FLAG	Serial data output to RH Processor
7	SIM_DATA_FLAG	Simulated data in use
6	SPARE2_FLAG	Bit definition is TBD
5	SPARE1_FLAG	Bit definition is TBD
4	DUMP_EEPROM	Dump - EEPROM in progress
3	DUMP_DATA_RAM	Dump - data ram in progress
2	DUMP_PROGRAM_RAM	Dump - program ram in progress
1	DUMP_PROGRAM_ROM	Dump - program prom in progress
0	DUMP_IO_MAP	Dump - io map in progress

3F06: DETECTOR STATUS REGISTER		
BIT	**MNEMONIC**	**DESCRIPTION**
14-15	<Not utilized>	
13	D2_CALIB_START	Det #2 calibration start
12	D2_PURGE_ENABLE	Det #2 gas purge enable
11	D2_PURGE_START	Det #2 gas purge start
10	D2_HV_ENABLE	Det #2 HV enable
9	D2_HV_SELCONVA	Det #2 HV select converter A
8	D2_HV_SELCONVB	Det #2 HV select converter B
7	D2_HV_FHLD_REL	Det #2 HV feedback hold(1)/release(0)
6	D1_CALIB_START	Det #1 calibration start
5	D1_PURGE_ENABLE	Det #1 gas purge enable
4	D1_PURGE_START	Det #1 gas purge start
3	D1_HV_ENABLE	Det #1 HV enable
2	D1_HV_SELCONVA	Det #1 HV select converter A
1	D1_HV_SELCONVB	Det #1 HV select converter B
0	D1_HV_FHLD_REL	Det #1 HV feedback hold(1)/release(0)

3F08: DUAL PORT CONTROL REGISTER		
BIT	**MNEMONIC**	**DESCRIPTION**
15	CAV	Command available bit
14	OVF	Overflow bit
13	SYN	One second sync bit
12	UPL	Memory upload bit
11	TAA	Time attitude data available bit
10	SRS	Soft reset bit
5-9	<Not utilized>	
0-4	WC	Word count (cmd buf/mem upload)

3F0A: DUAL PORT STATUS REGISTER		
BIT	**MNEMONIC**	**DESCRIPTION**
15	SDV	Science data available bit
14	CME	Command error bit
13	STE	Self test error bit
12	SOV	Science data overflow bit
10-11	TB0:1	Telemetry buffer select *TB1 TB0* 0 0 buffer 'A' 0 1 buffer 'B' 1 0 buffer 'C' 1 1 <illegal>
9	HAB	Housekeeping A/B bit (A=1)
8	HKA	Housekeeping data available bit
0-7	SC	State code bits (0:7) *(See appendix A for definition)*

3F0C: DUAL PORT SCIENCE REGISTER		
BIT	**MNEMONIC**	**DESCRIPTION**
12-15	MODE3:0	Telemetry Mode *M3:0* 0 SCIENCE DATA OFF 1 EVENT MODE 1 2 EVENT MODE 2 3 EVENT MODE 3 4 EVENT MODE 4 5 SPECTRAL MODE 6 <not assigned> 7 <not assigned> 8 LOW RATE SIM 9 HIGH RATE SIM 10-15 <not assigned>
0-11	WD0:11	Science Buffer Word count

3F0E: INTERRUPT ENABLE / EEPROM REGISTER		
BIT	**MNEMONIC**	**DESCRIPTION**
7	EEOFF	EEPROM power enable off(1) /on(0)
6	<Not utilized>	
5	WDTEN	Watch dog timer enable
4	PGSEL	EEPROM(1) /dual-port ram select
3	D2INTE	Detector 2 interrupt enable
2	D1INTE	Detector 1 interrupt enable
1	PG1	EEPROM page select (MSB)
0	PG0	EEPROM page select (LSB)

3F10: A/D STATUS & MUX REGISTER

BIT	MNEMONIC	DESCRIPTION
15	C2E	Command data 2 empty
14	C1E	Command data 1 empty
13	SR2	Science data 2 ready
12	SR1	Science data 1 ready
11	HR2	Housekeeping data 2 ready
10	HR1	Housekeeping data 1 ready
9	SHI	Science/housekeeping interrupt pending
8	ACC	A/D conversion complete
7	<Not utilized>	
6	OEP	Odd/even command parity
5	ULS	Upper/lower 8-bit ADC data select
0-4	MS	Mux address

3F12: A/D CONTROL REGISTER

BIT	MNEMONIC	DESCRIPTION
7	DR2	Detector #2 reset
6	DR1	Detector #1 reset
5	HE2	Detector #2 housekeeping int enable
4	SE2	Detector #2 science int enable
3	HE1	Detector #1 housekeeping int enable
2	SE1	Detector #1 science int enable
1	LT	Loopback test
0	ASC	ADC start conversion strobe

3F14: LAST PEP ADDRESS REGISTER

BIT	MNEMONIC	DESCRIPTION
0-15	last_pep_addr	Last science buffer location a PEP was written in event modes. The valid range is from 0x2041 to 0x3F60.

3F16: SCIENCE BUFFER POINTER

BIT	MNEMONIC	DESCRIPTION
0-15	p_sci_buf	Science buffer pointer. Points to either the base address of buffer A (0x2041) or buffer B (0x2AA1) in low rates. Always points to buffer A in high rate.

3F18: MILLISECOND COUNTER VALUE AT FRAMESYNC		
BIT	**MNEMONIC**	**DESCRIPTION**
0-15	ms_counter	Contains the value of the millisecond counter at framesync. Each tic equals 1.024 mS. For a one second sync, the value should be approx. 0x3D0. Time-out occurs when the count equals 0x432 or approx. 1.1seconds, and consequently initiates the framesync task by default.

3F1A: MINIMUM ELEMENTS IN QUEUE		
BIT	**MNEMONIC**	**DESCRIPTION**
0-15	q_ele_min	Indicates the minimum number of elements remaining in the queue. The range of values is 0 to 400 hex where the latter indicates an empty queue. (Queue depth is 1024 elements).

3F1C: INTERRUPT CONTROL & MASK REGISTERS		
BIT	**MNEMONIC**	**DESCRIPTION**
9-15	<Not utilized>	
4-8	ICNTL	ADSP-2100's interrupt control register.
0-3	IMASK	ADSP-2100's interrupt mask register.

3F1E: TIMER VALUE WHEN GPS RECEIVED		
BIT	**MNEMONIC**	**DESCRIPTION**
0-15	gps_ms_count	The value of the millisecond counter when the GPS time and attitude data was received by the DIB.

3F20: DIB COMMAND COUNT		
BIT	**MNEMONIC**	**DESCRIPTION**
0-15	dib_command_count	The number of valid commands received by the DIB since reset.

3F22: DIB LAST COMMAND		
BIT	**MNEMONIC**	**DESCRIPTION**
0-15	dib_last_command	The last command received and executed by the DIB.

3F24: DIB ERROR COUNT		
BIT	**MNEMONIC**	**DESCRIPTION**
0-15	dib_error_count	The number of erroneous commands received by the DIB.

3F26: DIB TOTAL EVENT COUNT		
BIT	**MNEMONIC**	**DESCRIPTION**
0-15	dib_total_evnt_count	The sum of the DIB generated event counts from both detectors. (The individual values are indicated in words 12 and 13 of the science parameter block).

3F28: SCIENCE BUFFER A WORD COUNT		
BIT	**MNEMONIC**	**DESCRIPTION**
0-15	bufa_wd_cnt	The number of words in science buffer A at framesync. In the low rate this word count will be zero on alternating buffers.

3F2A: SCIENCE BUFFER B WORD COUNT		
BIT	**MNEMONIC**	**DESCRIPTION**
0-15	bufb_wd_cnt	The number of words in science buffer B at framesync. In the low rate this word count will be zero on alternating buffers.

3F2C: SCIENCE BUFFER C WORD COUNT		
BIT	**MNEMONIC**	**DESCRIPTION**
0-15	bufc_wd_cnt	The number of words in science buffer C at framesync. In the low rate this word count will always be zero.

3F2E: ROUTINE ID		
BIT	**MNEMONIC**	**DESCRIPTION**
0-15	routine_id	Identifies the current routine executed (in real time). This is an extension to the state code of the status register, with less overhead. The routine identifiers are listed in the appendix B.

3F30: QUEUE ELEMENTS @ FRAMESYNC		
BIT	**MNEMONIC**	**DESCRIPTION**
0-15	q_ele_fs	Indicates the number of elements remaining in the queue at framesync. The range of values is 0 to 400 hex where the latter indicates an empty queue. (Queue depth is 1024 elements).

3F32: TIMER VALUE WHEN HOUSEKEEPING READY		
BIT	**MNEMONIC**	**DESCRIPTION**
0-15	hkp_ms_count	The value of the millisecond counter when the DIB housekeeping is ready to be transferred to the CPU/1553 processor.

3F34: FULL FRAME FLAG		
BIT	**MNEMONIC**	**DESCRIPTION**
0	full_frame_flag	When set high indicates that the event mode frame is full. No room exists to add additional Photon Event Packets (PEPs).

3F36: VEF/PH TIME THRESHOLD		
BIT	**MNEMONIC**	**DESCRIPTION**
0-5	cutoff_time	The maximum allowable amount of time difference between the arrival of the valid event flag and the received pulse height word. This range is programmable by the UTIMETHR command.

The following state code definitions describe bits 0-7 of the Dual Port Status Register located at debug address 3F0A.

APPENDIX A: STATE CODE DEFINITIONS		
STATE CODE	**GROUP**	**DEFINITION**
0x01	BOOT	UPLOAD_PROCESSING
0x02	BOOT	UPLOAD_SUCCESSFUL
0x05	BOOT	EEPROM_PROGRAM
0x06	BOOT	EEPROM_SUCCESS
0x07	BOOT	LOAD_FAIL_STATE
0x11	SELFTEST	SELFTEST_STATE
0x31	COMMAND	DUAL_PORT_STATE
0x32	COMMAND	CMD_DECODE_STATE
0x41	DUMP	DUMP_IO_STATE
0x42	DUMP	DUMP_PROM_STATE
0x43	DUMP	DUMP_PRAM_STATE
0x44	DUMP	DUMP_DRAM_STATE
0x45	DUMP	DUMP_EEPROM_STATE
0x51	FRAME SYNC & INIT	FRAME_SYNC_STATE
0x52	FRAME SYNC & INIT	INITIALIZE_STATE
0x53	FRAME SYNC & INIT	STEST_ERROR_STATE
0x54	FRAME SYNC & INIT	STANDBY_STATE
0x60	TELEMETRY MODES	FRAMEBLDR_STATE
0x61	TELEMETRY MODES	EVENT_MODE1_STATE
0x62	TELEMETRY MODES	EVENT_MODE2_STATE
0x63	TELEMETRY MODES	EVENT_MODE3_STATE
0x64	TELEMETRY MODES	EVENT_MODE4_STATE
0x65	TELEMETRY MODES	SPECTRAL_MODE_STATE
0x66	TELEMETRY MODES	HRATE_MODE_STATE
0x68	TELEMETRY MODES	LRATE_SIM_MODE_STATE
0x69	TELEMETRY MODES	HRATE_SIM_MODE_STATE
0x6A	TELEMETRY MODES	RH_PROC_STATE

The following routine ID definitions describe the Routine ID register located at debug address 3F2E.

APPENDIX B: ROUTINE ID DEFINITIONS		
ROUTINE ID	**MODULE**	**DEFINITION**
0x01	DAP_BGND.C	background( )
0x02	DAP_BGND.C	read_dp_status( )
0x03	DAP_BGND.C	write_dp_status( )
0x04	DAP_BGND.C	housekeep( )
0x05	DAP_BGND.C	build_hkp_frame( )
0x06	DAP_CMD.C	DualPort( )
0x07	DAP_CMD.C	CmdDecode( )
0x08	DAP_CMD.C	ExitRAM( )
0x09	DAP_DUMP.C	Memory_dump( )
0x0A	DAP_FRM.C	framesync( )
0x0C	DAP_FRM.C	enable_vef( )
0x0E	DAP_FRM.C	state_sts( )
0x0F	DAP_FRM.C	FrameBuilder( )
0x10	DAP_FRM.C	select_dump( )
0x11	DAP_FRM.C	TLMBuild( )
0x12	DAP_FRM.C	science_parm_blk( )
0x13	DAP_FRM.C	map_test_data( )
0x14	DAP_MAIN.C	main( )
0x15	DAP_PARM.C	initialize( )
0x16	DAP_PARM.C	init_variables( )
0x17	DAP_PARM.C	init_det_adm( )
0x18	DAP_PARM.C	init_sw_reg( )
0x19	DAP_PARM.C	init_circ_buffer( )
0x1A	DAP_PARM.C	init_buffers( )
0x1B	DAP_PARM.C	init_semaphores( )
0x1C	DAP_STST.C	SelfTest( )
0x1D	DAP_STST.C	ADC_Convert( )

3.2.2.6.4 CE Power Interface

The USA Detector Interface card shall require +5Vdc power at an maximum instantaneous peak current level of 1.024A and an average typical current level of 350mA.

3.2.2.6.5 Time Tag Interface

The USA Detector Interface shall receive science data at rates of up to 10,000 events per second from one detector or 20,000 events per second from two detectors simultaneously. Each event generates a valid event flag which shall be received from each detector. The USA Detector Interface card shall latch the time maintained by the GPS 1second reset signal independently for each detector. The CPU shall be capable of reading the 20-bit time value for each detector.

3.2.2.6.6 Analog/Digital Mux Card Interface

The USA Detector Interface card shall provide an interface to the Analog/Digital Mux card as defined in the specifications for the Analog/Digital Mux card.

3.2.2.6.7 Special Processor Interface

The USA Detector Interface card shall provide up to 16 TTL level signals to the special processor card slots as written directly by the CE bus processor, refer to section 3.2.2.6.3 for bit assignments.

3.2.2.6.8 Special Processor Data Interface

The USA Detector Interface card shall provide a data, clock, and strobe serial interface to the RH32 special processor in order to provide science data directly to the special processor. The clock rate shall be 1MHz and its timing shall be as defined in the following figure.

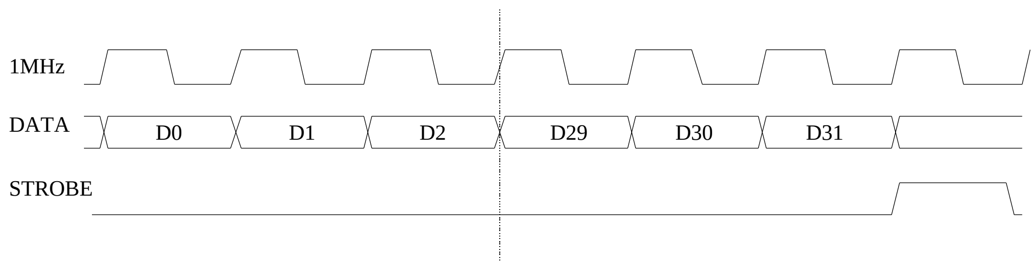


Figure 3.2.2.6.8-1 Data Interface Timing Diagram

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The data format of the serial stream shall be a function of the DIB’s science data mode. When the DIB is operating in an event mode, USCIMD1 to USCIMD4 or the RH processor mode, USCIMD6, the format shall be as identified in 3.2.2.6.8.1. When the DIB is operating in the spectral mode, USCIMD5, the format shall be as specified in section 3.2.2.6.8.2.

3.2.2.6.8.1 Event Queue Element Format

The format of special processor’s serial data when the DIB is operating in the event modes USCIMD1 to USCIMD4 or the RH special processor mode (USCIMD6) is shown in the table below.

SPECIAL PROCESSOR DATA INTERFACE EVENT QUEUE ELEMENT FORMAT			
BIT	FIELD NAME	BIT	FIELD NAME
0	<Not Assigned>	16	PEP Time, 2uS (time bit 1)
1	<Not Assigned>	17	PEP Time, 4uS (time bit 2)
2	<Not Assigned>	18	PEP Time, 8uS (time bit 3)
3	<Not Assigned>	19	PEP Time, 16uS (time bit 4)
4	<Not Assigned>	20	PEP Time, 32uS (time bit 5)
5	Vector Time, 2048uS (time bit 11)	21	PEP Time, 64uS (time bit 6)
6	Vector Time, 4096uS (time bit 12)	22	PEP Time, 128uS (time bit 7)
7	Vector Time, 8192uS (time bit 13)	23	PEP Time, 256uS (time bit 8)
8	Block Time, 16mS (time bit 14)	24	PEP Time, 512uS (time bit 9)
9	Block Time, 32mS (time bit 15)	25	PEP Time, 1024uS (time bit 10)
10	Block Time, 64mS (time bit 16)	26	Detector ID (0=Det1, 1=Det2)
11	Block Time, 128mS (time bit 17)	27	Pulse Height LSB (science bit 3)
12	Block Time, 256mS (time bit 18)	28	Pulse Height (science bit 4)
13	Block Time, 512mS (time bit 19)	29	Pulse Height (science bit 5)
14	Block Time, 1second (time bit 20)	30	Pulse Height (science bit 6)
15	Block Time, 2 second (time bit 21)	31	Pulse Ht Layer ID (0=layer1, 1=layer2)

Note that the low 3 bits of the pulse height (science bits 0,1 and 2) are not utilized in the event mode queue element.

3.2.2.6.8.2 Spectral Queue Element Format

The format of special processor's serial data when the DIB is operating in the spectral mode USCIMD5 is shown in the table below.

SPECIAL PROCESSOR DATA INTERFACE SPECTRAL QUEUE ELEMENT FORMAT			
BIT	FIELD NAME	BIT	FIELD NAME
0	Pulse Height LSB (science bit 0)	16	Period Offset (offset bit 0)
1	Pulse Height (science bit 1)	17	Period Offset (offset bit 1)
2	Pulse Height (science bit 2)	18	Period Offset (offset bit 2)
3	Pulse Height (science bit 3)	19	Period Offset (offset bit 3)
4	Pulse Height (science bit 4)	20	Period Offset (offset bit 4)
5	Pulse Height (science bit 5)	21	Period Offset (offset bit 5)
6	Pulse Height (science bit 6)	22	Period Offset (offset bit 6)
7	Pulse Ht Layer ID (0=layer1, 1=layer2)	23	Period Offset (offset bit 7)
8	<Not Assigned>	24	Period Offset (offset bit 8)
9	<Not Assigned>	25	Period Offset (offset bit 9)
10	<Not Assigned>	26	Period Offset (offset bit 10)
11	<Not Assigned>	27	Period Offset (offset bit 11)
12	<Not Assigned>	28	<Not Assigned>
13	<Not Assigned>	29	<Not Assigned>
14	<Not Assigned>	30	<Not Assigned>
15	Detector ID (0=Det1, 1=Det2)	31	<Not Assigned>

The period offset parameter identifies which of the 100 intervals (10mS each) that the pulse height value was received. (See section: 3.2.2.6.3.5.2 titled Spectral Mode) Specifically, the period offset is a value ranging from 0 to 99 (last period) that is multiplied by the interval buffer size, 24 words. The overall range is thus 0 to 2376 (99*24).

Note that all 8 bits of the pulse height are utilized in the spectral mode queue element.